A Nonvolatile Memory Device Made of a Ferroelectric Polymer Gate Nanodot and a Single-Walled Carbon Nanotube

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ABSTRACT We demonstrate a field-effect nonvolatile memory device made of a ferroelectric copolymer gate nanodot and a single-walled carbon nanotube (SW-CNT). A position-controlled dip-pen nanolithography was performed to deposit a poly(vinylidene fluoride-ran-trifluoroethylene) (PVDF-TrFE) nanodot onto the SW-CNT channel with both a source and drain for field-effect transistor (FET) function. PVDF-TrFE was chosen as a gate dielectric nanodot in order to efficiently exploit its bipolar chemical nature. A piezoelectric force microscopy study confirmed the canonical ferroelectric responses of the PVDF-TrFE nanodot fabricated at the center of the SW-CNT channel. The two distinct ferroelectric polarization states with the stable current retention and fatigue-resistant characteristics make the present PVDF-TrFE-based FET suitable for nonvolatile memory applications.

KEYWORDS: ferroelectric polymer nanodot · carbon nanotube · field-effect transistor · nonvolatile memory device

In the past decade, carbon nanotubes (CNTs) have been extensively investigated for their applications to various fields, including field-effect transistors (FETs), electron field emitters, and hydrogen storage.[1−8] Both single-walled CNTs (SW-CNTs) and multiwalled CNTs (MW-CNTs) show high current-carrying capabilities and excellent carrier mobility with a small band gap.[6] A SW-CNT is a seamlessly wrapped single graphene sheet formed into a cylindrical tube, and a MW-CNT is composed of multiple rolled layers of graphene. Both types of CNTs have high Young's moduli and tensile strengths with excellent flexibilities, demonstrating their potentials as candidates for channel materials of the next generation FETs.[7]

Ferroelectric FETs (FeFETs) are nonvolatile random access memory (NVRAM) architectures with a small size and a low operating voltage coupled with fast operation.[8−11] Though Pb-based perovskites, such as $Pb(Zr,Ti)O_3$ (PZT), exhibit excellent ferroelectric properties, lead toxicity is a major disadvantage for their applications to FeFETs.[12,13] Therefore, many researchers have developed lead-free ferroelectrics.[14−18] Among these, ferroelectric copolymers such as poly(vinylidene fluoride-ran-trifluoroethylene) (PVDF-TrFE) have been attractively studied because of their low crystallization temperatures, flexibilities, and nontoxicities.[15−17]

Ferroelectric nanostructures have been fabricated by exploiting various techniques, including anodizing electron-beam lithography, aluminum oxide nanotemplates, and a Si mold for PVDF-TrFE nanodots.[17,19,20] Currently, CNT-based FETs combined with ferroelectric nanostructures do not achieve a truly nanoscale dimension. Therefore, it is highly desirable to develop a new fabrication technique that can readily handle nanostructures with positional controllability. Dip-pen nanolithography (DPN) technology based on scanning probe microscopy enables the production and handling of various nanostructure materials, including polymers and semiconductors.[21−23] In particular, a recently reported DPN of $PbTiO_3$ nanodots provided the production and handling of a ferroelectric nanostructure at a desired position with nanometer-scale accuracy.[23] In spite of extensive research efforts on DPN, however, it has not been successfully implemented in the practical realization of a nanoscaled nonvolatile memory device.

In the present study, a nanometer-scale NVRAM device made of a ferroelectric PVDF-TrFE nanodot and a SW-CNT channel is demonstrated by suitably exploiting the DPN method. The PVDF-TrFE nanodot was chosen as a gate dielectric to efficiently exploit its bipolar chemical nature. In addition, a polymer gate rather than an inorganic oxide gate was adopted by considering its chemical affinity (*i.e.*, low interfacial tension) toward the CNT channel with a

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Received for review August 24, 2010 and accepted October 28, 2010.

Published online November 4, 2010. 10.1021/nn1021296

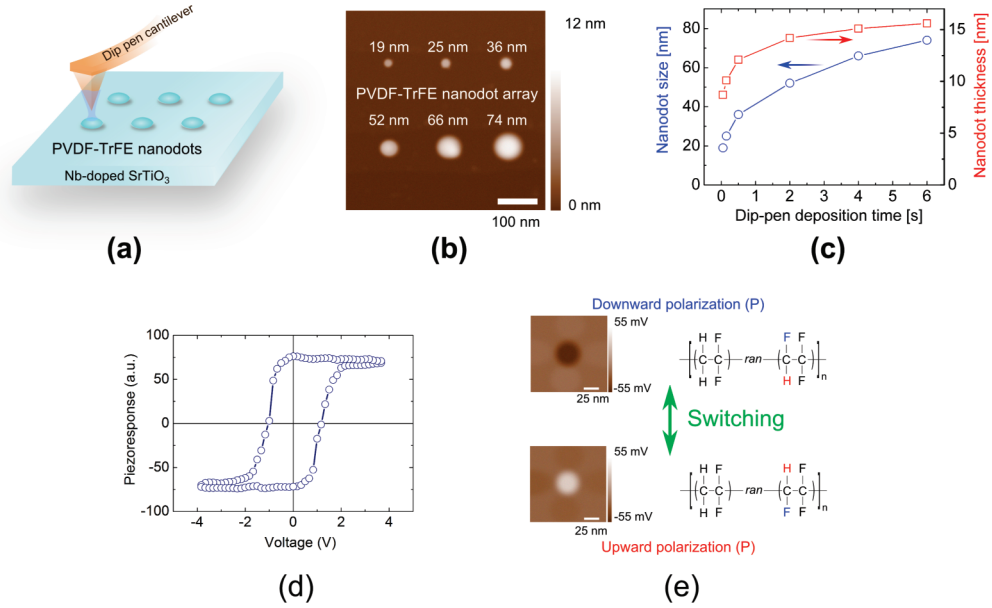

Figure 1. PVDF-TrFE nanodots prepared by dip-pen nanolithography (DPN). (a) Fabrication of PVDF-TrFE nanodots on a Nb-doped $SrTiO_3$ substrate using the DPN method. (b) AFM image of various PVDF-TrFE nanodots formed on a Nb-doped $SrTiO_3$ substrate. (c) Nanodot size (diameter and thickness) plotted as a function of the dip-pen deposition time. (d) Piezoelectric hysteresis loop of the PVDF-TrFE-gate nanodot with a diameter of 19 nm. Piezoelectric characteristics were examined by exploiting piezoelectric force microscopy (PFM). (e) Two PFM images of the PVDF-TrFE-gate nanodot with a diameter of 19 nm. The top and bottom PFM images correspond to the downward and upward polarizations, respectively. A bipolar chemical nature of PVDF-TrFE is schematically depicted in the right-hand-side figure using two distinct orientations of the proton (H^+) in a TrFE unit.

minimum concentration of interfacial defects.[15] By fully utilizing the nanometer-scale controllability of the DPN method,[23] we have successfully formed a PVDF-TrFE nanodot gate precisely at the center of the SW-CNT channel. This polymer-gate-based FeFET shows desirable memory effects that are suitable for NVRAM applications.

RESULTS AND DISCUSSION

Figure 1a schematically depicts the formation of polymer nanodots on a Nb-doped $SrTiO_3$ substrate by the DPN method. PVDF-TrFE nanodots were made by serial procedures composed of dipping the precursor sol, drying, and annealing at 140 °C for 1 h.[15−17,24,25] Figure 1b shows an atomic force microscope (AFM) image of the DPN-formed nanodots with various diameters. The dimension (diameter, thickness) of the nanodot is precisely controlled by adjusting the dip-pen deposition time (Figure 1c). A piezoelectric hysteresis loop of the nanodot having a diameter of 19 nm demonstrates the switching of ferroelectric polarization (Figure 1d). Because of a bipolar chemical nature of PVDF-TrFE polymer, the polarization switching can be achieved by swapping the fluorine anion (F^-) with the proton (H^+) counterpart in a TrFE unit (Figure 1e).

The DPN fabrication of the PVDF-TrFE-based FeFET is schematically depicted in Figure 2. A source and drain were prepared from gold electrodes at both ends of the SW-CNT channel using an electron-beam lithography technique (Figure 2a). Then, a PVDF-TrFE nanodot was suspended at the center of the CNT channel by dip-pen lithography (Figure 2b). We subsequently embodied a polymer nanodot-based CNT-FeFET memory device in which all of the components were integrated into a single piece within a nanometer scale (Figure 2c). Figure 2d presents an AFM image of the PVDF-TrFE-deposited SW-CNT. In Figure 2d, a Au-metal gate was fabricated on the PVDF-TrFE-gate nanodot using the DPN method. A fairly straight SW-CNT was observed on the SiO_2/Si substrate. In addition, well-aligned terraces were observed, indicating an atomically flat surface of the SiO_2/Si substrate with the rms (root-mean-square) roughness of less than 0.1 nm. The PVDF-TrFE nanodot with a diameter of 28 nm was formed exactly at the center of the SW-CNT, demonstrating nanometer-scale controllability of the present DPN technology. The surface line profile presented in Figure 2e indicates that the thickness of the PVDF-TrFE nanodot is approximately 9.2 nm. This nanometer-sized gate has further applications to high-density data storage with a storage capacity of ~Tbit/inch^2 (refs 8 and 17).

The ferroelectric properties of the PVDF-TrFE copolymer nanodot were investigated by utilizing piezoelectric force microscopy (PFM). Prior to the PFM measurement, the ferroelectric polymer nanodot was electrically polarized by applying a bias voltage of ±5 V. PFM images of the ferroelectric polymer nanodot were obtained for both upward and downward polarizations (before depositing the Au-metal gate onto the polymer nanodot). During the switching process, a bias voltage of ±5 V was applied through the conducting PFM tip by simultaneously grounding the source, drain, and

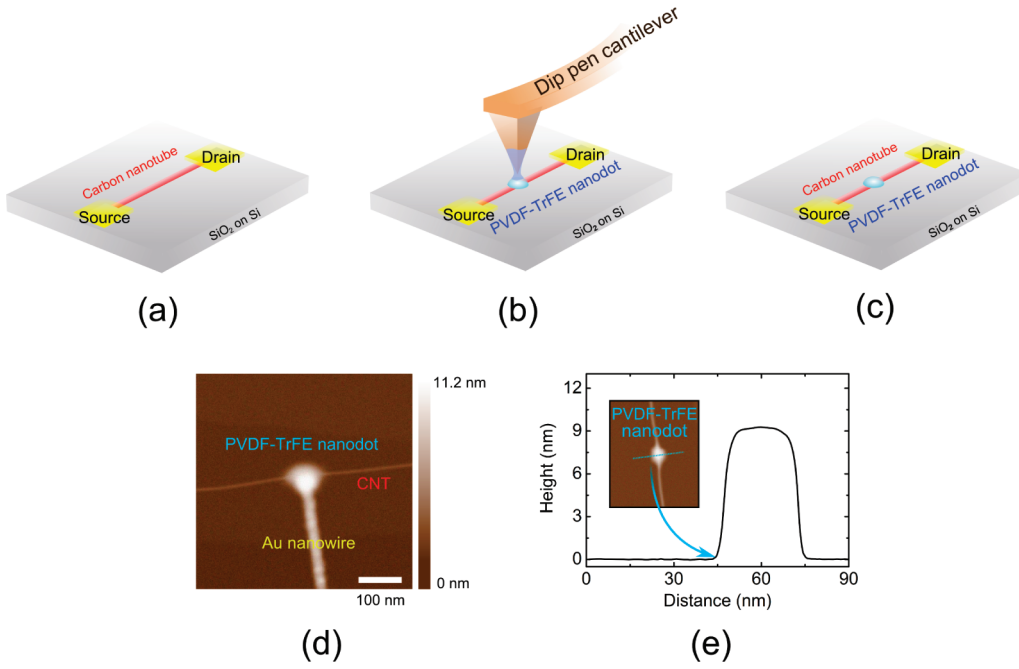

Figure 2. Schematic drawings on the DPN fabrication of the PVDF-TrFE-based FeFET device and associated AFM images. (a) Preparation of a source and drain at both ends of the SW-CNT channel deposited onto a SiO_2/Si substrate. (b) Formation of the PVDF-TrFE-gate nanodot using the DPN method. (c) Ferroelectric FET composed of the SW-CNT channel and the PVDF-TrFE-gate nanodot suspended at the center of the CNT channel. (d) AFM image of the CNT-based nonvolatile memory device, entirely composed of nanostructured elements. (e) Surface line profile across the PVDF-TrFE nanodot region.

Si substrate. In the PFM image, the upward polarization (Figure 3a) is clearly distinguished from the downward polarization (Figure 3b). The piezoelectric hysteresis loop presented in Figure 3c demonstrates a switching of the ferroelectric polarization with a coercive voltage of ~1.2 V. The coercive voltage of the PVDF-TrFE film having the same thickness of ~10 nm (thus, coercive field) is approximately 2.1 V and, thus, is substantially higher than that of the PVDF-TrFE nanodot (Supporting Information). A Kelvin force microscopy (KFM) image of the nanodot for the upward polarization (Figure 3d) is clearly distinguished from that

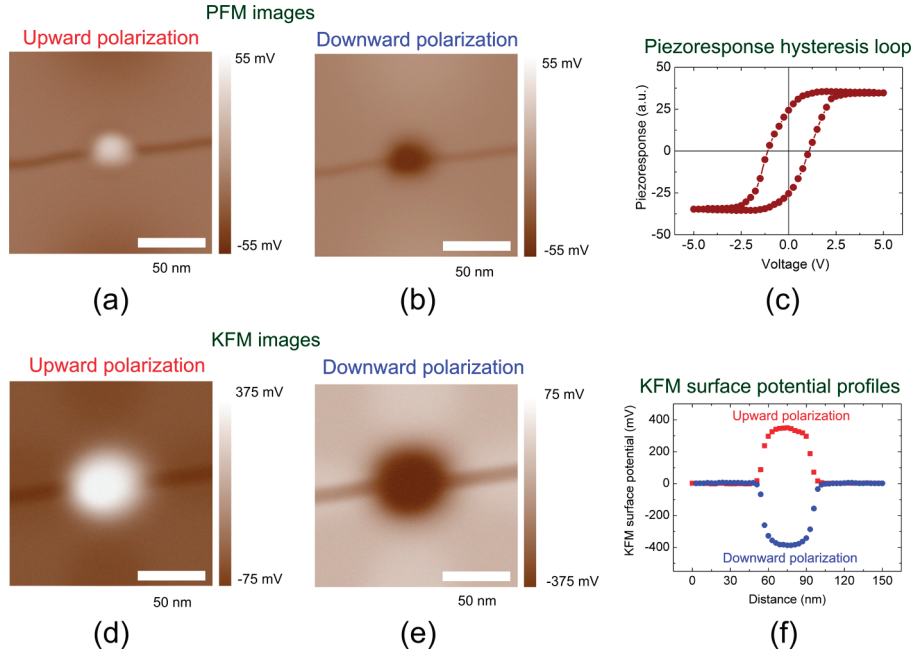

Figure 3. PFM and KFM data of the PVDF-TrFE-gate nanodot deposited onto the SW-CNT channel. A PFM image for the upward polarization (a) is clearly distinguished from that for the downward polarization (b). (c) Piezoelectric hysteresis loop of the PVDF-TrFE-gate nanodot demonstrating the switching of the ferroelectric polarization at an applied bias voltage of ~1.2 V. KFM images of the PVDF-TrFE nanodot region are presented for both (d) upward and (e) downward polarizations. (f) Measured KFM surface potential plotted as a function of the lateral distance along the CNT channel.

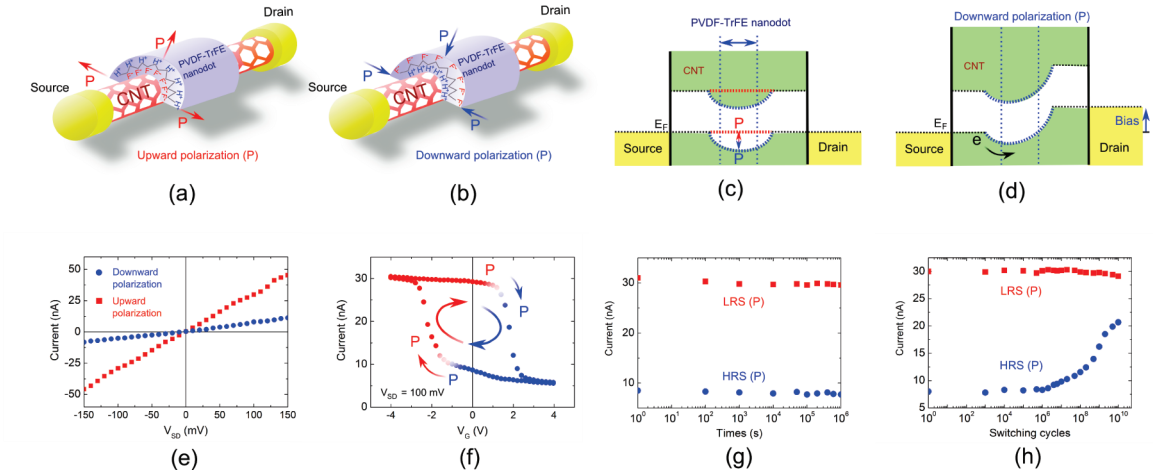

Figure 4. NVRAM characteristics of the PVDF-TrFE-gate FET memory device. Schematic drawings that show a bipolar chemical nature of the PVDF-TrFE-gate nanodot: (a) upward and (b) downward polarizations. (c) Band diagram that schematically illustrates the operation principle of the PVDF-TrFE-gate-based FET. Tunneling contacts between the SW-CNT and the Au electrodes are indicated by two black vertical lines. (d) Schematic band diagram illustrating the effect of a positive bias field on the band structure across the CNT channel. (e) Measured current values plotted as a function of the source−drain voltage (V_{SD}) for both upward and downward polarizations. (f) $I_{SD}-V_G$ transfer curve of the PVDF-TrFE-based FET memory device at a fixed value of V_{SD} = 100 mV. (g) Two retained I_{SD} states plotted as a function of the relaxation time. (h) Fatigue-test result of the PVDF-TrFE-based FET memory device.

of the downward polarization (Figure 3e). The measured KFM surface potential is plotted in Figure 3f as a function of the lateral distance along the CNT channel. The KFM surface potential clearly splits into two distinct values (+380 and −400 mV) at the PVDF-TrFE nanodot region, which demonstrates the polarization switching between the downward and upward states.

The bipolar chemical nature of the PVDF-TrFE gate is schematically depicted in Figure 4a,b for the two distinct polarization states. The electronegative fluorine anions (F^-) in the PVDF-TrFE cover the CNT surface in the upward polarization (Figure 4a), whereas the protons (H^+) are oriented toward the CNT surface in the downward polarization (Figure 4b). In Figure 4a,b, the upward polarization corresponds to a negative gate bias, while the downward polarization corresponds to a positive bias voltage.[15] PVDF-TrFE was deliberately chosen in order to exploit its bipolar chemical nature for controlling the gate current *via* the bias voltage. Figure 4c,d schematically describes the operation principle of the present PVDF-TrFE-gate-based FeFET. Due to a difference in the work functions between the CNT and the PVDF-TrFE gate dielectric, the downward polarization (+V gate; marked with a blue arrow) induces a band bending (blue dots) at the gate region (Figure 4c), which leads to a highly resistive state. Alternatively, the upward polarization (−V gate; red arrow) effectively flattens the band, resulting in a metal-like behavior.[1] An applied positive bias voltage does build up a chemical potential gradient between the source and drain (Figure 4d). This consequently suppresses the barrier or the degree of band bending slightly, which results in an increased current density under a positive bias field.[1]

The NVRAM characteristics of the present polymer-gate FET memory device were experimentally examined. Figure 4e presents the measured current values plotted as a function of the source−drain voltage ($I-V_{SD}$ curve) for both upward and downward polarizations of the ferroelectric PVDF-TrFE nanodot. In the measurement, the conducting AFM tip was entirely removed after electrically polarizing the gate nanodot. As shown in Figure 4e, the PVDF-TrFE-gate FET exhibits two distinct linear $I-V_{SD}$ curves with different slopes, distinguishing the high resistance state (HRS) from the low resistance state (LRS).[1,5] Figure 4f presents the $I_{SD}-V_G$ transfer curve which indicates a p-type Schottky barrier in the present FeFET. The hole carrier mobility is estimated to be about 150 $cm^2\ V^{-1}\ s^{-1}$ (refs 1 and 2). On the basis of the upward polarization (*i.e.*, −V gate), the polymer-gate FET exhibits an LRS in the $I-V_{SD}$ curve with a resistance value of approximately 3.3 MΩ. On the contrary, the FET for the downward polarization (+V gate) is characterized by a HRS with a resistance as high as ∼13.7 MΩ. These two distinct resistivity characteristics depending on the bias voltage can exploit the present PVDF-TrFE-gate nanodot structure for applications to CNT-based NVRAM devices in which all of the components are integrated into a single nanometer-sized piece. In addition, the $I-V_{SD}$ current of the HRS (downward polarization) can be significantly reduced by adopting a PVDF-TrFE-gate nanodot with a diameter greater than 28 nm (Supporting Information).

To assess the device reliability of the PVDF-TrFE-based FET toward NVRAM applications,[10] we have examined data retention and electrical fatigue characteristics. The V_{SD} value was fixed at 100 mV to evaluate the source−drain current (I_{SD}). As shown in Figure 4g, the

bistable currents of the LRS and HRS are well retained up to 10^6 s, demonstrating a desirable retention property of the present FET device. The fatigue resistance is another important criterion in NVRAM applications as it represents a resistance against the I_{SD} degradation which arises from repeated writing and erasing operations. The fatigue resistance characteristics were examined using a triangular bipolar bias of 5 V at 1 kHz as the repetition switching bias. Though the current value of the HRS increases rather rapidly at a certain critical value of the switching cycle ($\sim 10^8$), the PVDF-TrFE-based FET exhibits acceptable memory characteristics (*i.e.*, two separate current states) up to $\sim 10^{10}$ switching cycles (Figure 4h).

CONCLUSIONS

A nonvolatile random access memory (NVRAM) device made of a ferroelectric polymer-gate nanodot and a single-walled CNT was demonstrated. By exploiting the DPN method, a PVDF-TrFE polymer nanodot was formed at a desired position on a CNT channel. This polymer-gate nanodot enables us to establish two distinct resistivity characteristics depending on its ferroelectric polarization, with the low and high resistance states corresponding to the upward and downward polarizations, respectively. The bistable currents with a desirable retention property and the fatigue resistance make the present PVDF-TrFE-based FET suitable for nonvolatile memory applications.

METHODS

A nonvolatile memory device was fabricated to have a single-walled CNT and a gate ferroelectric copolymer, poly(vinylidene fluoride-ran-trifluoroethylene) (PVDF-TrFE). For this purpose, SiO_2/Si substrates were first prepared by the Radio Corporation of America (RCA) cleaning and thermal oxidation. The thickness of the thermally grown SiO_2 layer was estimated to be 20 nm. The SW-CNTs prepared by plasma-enhanced chemical vapor deposition were sonicated into a dispersion using dichloroethane. A source and drain made of gold electrodes were prepared at both ends of the SW-CNT channel using an electron-beam lithography technique. A PVDF-TrFE nanodot was suspended precisely at the center of the CNT channel by dip-pen lithography (DPN) of a randomly copolymerized solution made of 70/30 mol % polyvinylidene fluoride and polytrifluoroethylene. To elaborate the DPN process, an atomically flat SiO_2/Si substrate with well-aligned terraces was used. After the deposition using a sharp Si_3N_4 DPN tip with a radius less than 10 nm, the precursor sol nanodots were slowly dried for several days at room temperature. The polymer nanodot was subsequently annealed at 140 °C for 1 h. Finally, a polymer-gate-based CNT-FeFET device in which all of the components were integrated into a single nanometer-sized piece was obtained.

Morphological features of the gate nanodots were examined using an atomic force microscope equipped with a sharp Si_3N_4 tip, with its radius less than 10 nm. PFM and KFM studies were performed to investigate the ferroelectric switching characteristics of the nanodot by switching and subsequent reading of the ferroelectric domain under an applied electric field. A platinum-coated Si_3N_4 conducting tip (tip radius $\sim$20 nm, tip height 15 μm, resonance frequency $\sim$80 kHz, and spring constant $\sim$0.65 N/m; MIKROMASCH) and a constant scanning speed of 50 nm/s were used in PFM and KFM measurements. A platinum-coated conducting PFM tip was used in the PFM measurements. The channel current was measured as a function of the source−drain voltage ($I-V_{SD}$ curve) for both upward and downward polarizations of the ferroelectric PVDF-TrFE nanodot. The bistable currents were measured as a function of the switching cycle for the two distinct resistance states (HRS and LRS) by fixing the V_{SD} value at 100 mV.

Acknowledgment. This work was supported by the Brain Korea 21 Project 2010 and by the Korea Research Foundation Grant under Contract No. KRF-2008-313-C00309. This research was also supported by the WCU (World Class University) program through the Korea Research Foundation funded by the Ministry of Education, Science and Technology (Grant No. R31-2008-000-10059-0), Republic of Korea.

Supporting Information Available: Ferroelectric hysteresis loop of the PVDF-TrFE polymer thin film, schematic drawings that illustrate the fabrication of the Au-metal gate on the polymer gate nanodot, and $I-V_{SD}$ curves of the CNT-based nonvolatile memory device. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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